Refine Search

Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Search Results -

Terms	Documents
L11 same test$ same wafer	2

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L13

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, August 03, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L13	L11 same test$ same wafer	2	L13
L12	L11 and l9	1	L12
L11	L1 same l2	571	L11
L10	L9 and l1	83	L10
L9	(david near1 ton)[xa,xp]	458	L9
L8	L1 same l2 same (bist or bisr)	0	L8
L7	(4703436| 5256578)![pn]	4	L7
L6	L5 same memory	6	L6
L5	L4 same test$	68	L5
L4	L3 same l2 same l1	96	L4
L3	associat$	2505635	L3

L2	(fail$ near1 test) or (result adj information)	20555	L2
L1	(identif$ near device) or id	1785322	L1

END OF SEARCH HISTORY

L6: Entry 1 of 6 File: USPT Nov 1, 1994

DOCUMENT-IDENTIFIER: US 5360747 A
** See image for Certificate of Correction **
TITLE: Method of reducing dice testing with on-chip identification

Detailed Description Text (6):
Referring back to FIG. 4B, during step 411, all wafers are subjected to predetermined, adverse conditions to accelerate discharge of the memory cells on the wafers. Then, in step 412 of second wafer sort 430, the probe reads the ID cells of the first electronically inked die on the wafer. For example, the probe examines the ID cells 7 (FIG. 2) on die 200 (the first electronically inked die) to access the file associated with the particular wafer on which die 200 is located, i.e. wafer W2. The file associated with wafer W2, i.e. file 2, is accessed in step 413. The probe, after reading the first location in the file, proceeds directly to the first "good" die (as determined in first wafer sort 400) on the wafer in step 414. Note that the first good die in this example is, in fact, die 200. Die 200 is then tested in step 415. If die 200 fails this test, the die is rejected, whereas if die 200 passes the test, the die is acceptable for the packaging process.

L5: Entry 4 of 68 File: USPT Mar 9, 2004

DOCUMENT-IDENTIFIER: US 6703573 B2
TITLE: Method for sorting integrated circuit devices

Detailed Description Text (5):
ICs that pass the test step 22 are typically shipped to customers, while those that fail the test step 22 are directed to the reject bin 12. At a point in time when test standards of the test step 22 have been relaxed as described above, the ICs in the reject bin 12 are sorted in a sort step 26 by reading the fuse ID of each IC, accessing the test data 24 associated with the fuse ID, and comparing the accessed test data 24 with the relaxed test standards. Those ICs that fail even the relaxed test standards are directed back to the reject bin 12, while those ICs that pass the relaxed test standards are typically shipped to customers. The method 10 thus successfully culls shippable ICs from the reject bin 12 without retesting the ICs.